Abstract

[0083] A method and apparatus for estimating burn-in time for integrated circuit die on a wafer employs a reliability testing structure placed in a scribe line area of a wafer to permit improved estimation of burn-in time for integrated circuit on a wafer. Each reliability testing structure has a plurality of evaluation device structures formed on the substrate. Groups of the evaluation device structures are stacked on the surface of the substrate. The device structures are created to permit evaluation of one of a plurality of failure mechanisms of the integrated circuit. A forcing input pad and a sensing output pad are connected through a selection circuit to at least one of the evaluation devices. The selection circuit selects which of the evaluation devices are to receive a stimulus and to transmit a response. The stimulus is activated and the substrate is then stressed. Each selected evaluation device structure is examined for failure and the hazard rate for each failure mechanism of the integrated circuit is determined and from the hazard rate the burn-in time for the integrated circuit is calculated.